Daniel Kostecki

thi nguyen

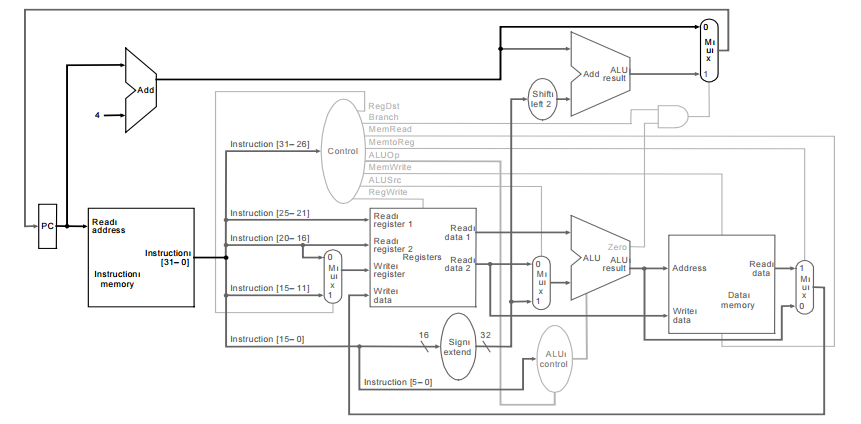
sonia leonato soiras

**CS385 – Computer Architecture**

**Project report #1**

1. **The names of the team members and the tasks that each one accomplished.**
2. **A detailed description of the instruction set architecture of the current version of the CPU (instruction codes, formats, meaning).**
3. **Logic diagrams or truth tables (for non-gate level designed modules) of the CPU and each of its major components (ALU, regfile, control unit) with labels for all components and data/control signals corresponding exactly to the modules, input/outputs and wire names used in the Verilog code.**

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Instr** | **RegDst** | **ALUSrc** | **MemReg** | **RegWrite** | **MemRead** | **MemWrite** | **Branch** | **ALUOp1** | **ALUOp2** |
| **Rtype** | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 |
| **addi** | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |



1. **The Verilog source code including detailed comment for each module defined or used.**
2. **Test results showing the correct functioning of the CPU by running a test program. The source and the machine language translation of the program must be included too.**